

## CLAIMS

What is claimed is:

1           1. A method for encoding instructions as a very long instruction word for processing  
2           in a plurality of computation units that reduces instruction memory requirements in a  
3           processing system, the method comprising the steps of:

4           (a)     determining at which stages of instruction processing that an instruction code  
5           needs to be executed; and

6           (b)     utilizing an enable signal of the instruction code to direct execution during  
7           the determined stages by enabling storage operations for the instruction code.

8           2. The method of claim 1 where the instruction code is associated with one of a  
9           plurality of computation units.

10          3. The method of claim 2 further comprising the step of (c) utilizing an action signal  
11          of the instruction code to execute each instruction when.

12          4. The method of claim 3 wherein utilizing an enable signal step (b) further  
13          comprises the step of (b1) encoding a chosen number of bits of the instruction code as the  
14          enable signal.

1           5. The method of claim 4 wherein the utilizing an action signal (c) further comprises  
2 the step (c1) encoding a remaining number of bits of the instruction code as the action  
3 signal.

1           6. The method of claim 3 wherein utilizing the enable signal and action signal for  
2 the instruction code avoids utilizing NOP (no operation) instruction codes in the very long  
3 instruction word.

1           7. A method for forming a very long instruction word in a processing system, the  
2 method comprising the steps of:

3           (a)     encoding each instruction code of the very long instruction word as an enable  
4 signal and an action signal to collapse instruction fields in the very long instruction word;  
5 and

6           (b)     associating each instruction code with a computation unit.

7           8. The method of claim 7 further comprising the step of (c) utilizing the enable  
2 signal to control storage operations when the action signal of each instruction is processed in  
3 the computation unit.

1           9. The method of claim 8 wherein the utilizing the enable signal (step c) occurs  
2 during each stage of processing.

1           10. The method of claim 9 wherein the utilizing the enable signal step (c) occurs  
2 during a loop stage of processing.

1           11. The method of claim 7 wherein the associating step (b) further comprises the  
2 step of (a1) associating based on a dataflow graph.

1           12. The method of claim 7 wherein the encoding step (a) further comprises the step  
2 of (a1) scheduling the very long instruction word for parallel processing.

1           13. A system for encoding instructions as a very long instruction word for  
2 processing that reduces instruction memory requirements in a processing system, the system  
3 comprising:

4           a plurality of computation units; and

5           a controller for controlling the plurality of computation units, wherein the controller  
6 determines at which stages of instruction processing that an instruction code needs to be  
7 executed and utilizes an enable signal of the instruction code to direct execution during the  
8 determined stages by enabling storage operations for the instruction code.

1           14. The system of claim 13 wherein the controller further utilizes an action signal of  
2 the instruction code for execution of each instruction in one of the plurality of computation  
3 units.

1                    15. The system of claim 14 wherein the controller further encodes a chosen number  
2 of bits of the instruction code as the enable signal.

1                    16. The system of claim 15 wherein the controller further encodes a remaining  
2 number of bits of the instruction code as the action signal.

1                    17. The system of claim 13 further comprising an adaptable computing engine, the  
2 adaptable computing engine including the plurality of computation units and the controller.